IN THE CLAIMS

1. (Currently amended) A method of fabricating a non-volatile semiconductor memory device, comprising:

(a) forming a device isolation layer in a substrate;

(b) forming a low-voltage gate insulating layer in at least a peripheral low-voltage region of the substrate, and forming a high-voltage-type gate insulating layer in at least a peripheral high-voltage region of the substrate;

(c) stacking a first conductive layer over substantially ~~the~~ an entire surface of the substrate;

(d) removing the first conductive layer in a cell array region to expose the substrate; and

(e) sequentially forming a triple layer and a second conductive layer over substantially the entire surface of the exposed substrate in the cell array region, the triple layer including a tunneling insulating layer, a charge storage layer, and a blocking insulating layer.

2. (Currently amended) A method of fabricating a non-volatile semiconductor memory device, comprising:

(a) forming a device isolation layer in a substrate;

(b) forming a low-voltage gate insulating layer in at least a peripheral low-voltage region of the substrate, and forming a high-voltage gate insulating layer in at least a peripheral high-voltage region of the substrate;

(c) stacking a first conductive layer over substantially ~~the~~ an entire surface of the substrate;

(d) removing a portion of the first conductive layer in the cell array region to expose a region of the substrate;

(e) sequentially forming a triple layer and a second conductive layer on the resulting structure including the first conductive layer and the exposed region of the substrate, the triple layer including a tunneling insulating layer, a charge storage layer, and a blocking insulating layer;

(f) patterning a substrate where the second conductive layer is formed, whereby forming a cell gate pattern in the cell array region and forming high-and low-voltage-type gate patterns in the peripheral high-and low-voltage regions, respectively;

(g) removing a portion of the second conductive layer and a portion of the triple layer of the respective high-and low-voltage-type gate patterns to form a butting region exposing the first ~~polysilicon~~ conductive layer;

(h) forming and patterning an interlayer insulating layer over substantially the entire surface of the substrate to form contact holes including a butting contact hole extending over the butting region; and

(i) forming a contact plug to fill the contact holes.

3. (Currently amended) The method as claimed in claim 2, wherein in the step (b), the gate insulating layer for a high voltage is formed in a resist region,

wherein in the step (f), a resistor pattern is formed in the resist region,

wherein in the step (g), the second conductive layer and the triple layer are removed in ~~the~~ a contact region of the resistor pattern, and

wherein in the step (h), contact holes are formed within the contact region in the resistor pattern ~~so that they are not connected to a high-conductivity layer~~.

4. (Original) The method as claimed in claim 2, further comprising forming an insulating spacer on sidewalls of the patterns.

5. (Original) The method as claimed in claim 2, wherein the second conductive layer is formed by sequentially stacking a conductive layer of silicon and another conductive layer of metal.

6. (Currently Amended) The method as claimed in claim 5, wherein in the step (a), a trench-type device isolation layer is formed in the resist region,

wherein in the step (f), a resistor pattern is formed in the resist region,

wherein in the step (g), the conductive layer of metal is removed ~~in all regions of the conductive~~from the resistor pattern, and

wherein in the step (h), a contact hole is formed to expose the ~~polysilicon~~ conductive layer of the silicon from the resistor pattern.

7. (Currently amended) A method of fabricating a non-volatile semiconductor memory device, comprising:

(a) forming a low-voltage gate insulating layer in at least a peripheral low-voltage region of a substrate, and forming a high-voltage gate insulating layer in at least a peripheral high-voltage region of the substrate;

(b) stacking a first conductive layer on an entire surface of the substrate;

(c) removing the first conductive layer in a cell array region to expose the substrate;

(d) sequentially forming a triple layer and a second conductive layer on an entire surface of the ~~exposed~~ substrate ~~in~~ where the first conductive layer in the cell array region is removed, the triple layer including a tunneling insulating layer, a charge storage layer, and a blocking insulating layer;

(e) forming a trench-type device isolation layer on a substrate where the second conductive layer is formed;

(f) forming a high-conductivity layer on a substrate where the device isolation layer is formed;

(g) patterning a substrate where the high-conductivity layer is formed, whereby forming a cell gate pattern in the cell array region and forming high-and low-voltage gate patterns in the peripheral high-and low-voltage regions, respectively;

(h) removing the ~~low resist conductive~~ high-conductivity layer, the second conductive layer, and the triple layer of the respective high-and low-voltage-type gate patterns to form a butting region exposing the first ~~polysilicon~~ conductive layer;

(i) forming and patterning an interlayer insulating layer on an entire surface of the substrate to form contact holes including a butting contact hole extending over the butting region; and

(j) forming a contact plug to fill the contact hole.

8. (Currently amended) The method as claimed in claim 7, where in the step (a), the gate insulating layer is formed in a resist region,

wherein in the step (g), a resistor pattern is formed in the resist region,

wherein in the step (h), the high-conductivity layer, the second conductive layer, and the triple layer are removed in ~~the~~ a contact region of the resistor pattern, and

wherein in the step (i), a contact hole is formed ~~to extend over only~~ in the contact region of the resistor pattern.

9. (Original) The method as claimed in claim 7, further comprising forming an insulating spacer on each of the sidewalls of the patterns formed in the step (g).

10. (Original) The method as claimed in claim 7, wherein the high-conductivity layer is formed by sequentially stacking a conductive layer of silicon and another conductive layer of metal.

11. (Currently Amended) The method as claimed in claim 10, wherein in the step (e), a trench-type device isolation layer is formed in the resist region,

wherein in the step (f), a resistor pattern is formed in the resist region,

wherein in the step (g), the conductive layer of metal is removed ~~in all regions of~~ from the ~~conductive~~ resistor pattern, and

wherein in the step (h), a contact hole is formed to expose the ~~polysilicon~~ conductive layer of the silicon from the resistor pattern.

12. (Currently amended) A method of fabricating a non-volatile semiconductor memory device, comprising:

(a) forming a device isolation layer in a substrate;

(b) forming a low-voltage-type gate insulating layer in at least a peripheral low-voltage region of the substrate, and forming a high-voltage type gate insulating layer in at least a peripheral high-voltage region of the substrate;

(c) stacking a first conductive layer on an entire surface of the substrate;

(d) removing the first conductive layer in the cell array region to expose the substrate;

(e) sequentially forming a triple layer and a second conductive layer over substantially ~~the~~ an entire surface of the ~~exposed~~ substrate where the first conductive layer in the cell array region is removed, the triple layer including a tunneling insulating layer, a charge-storage layer, and a blocking insulating layer;

(f) patterning a substrate where the second conductive layer is formed, thereby removing the second conductive layer and the triple layer in a removal region including the peripheral low-and high-voltage regions;

(g) forming a high-conductivity layer on an entire surface of the substrate; and

(h) patterning a substrate where the ~~second conductive~~high-conductivity layer is formed, whereby forming a cell gate pattern in the cell array region and forming high-and low-voltage-type gate patterns in the peripheral high-and low-voltage regions, respectively.

13. (Currently amended) The method as claimed in claim 12, further comprising:

(i) forming and patterning an interlayer insulating layer over the substantially the entire surface of the substrate to form a contact ~~holes including contact~~ holes exposing the high-conductivity layer; and

(j) forming a contact plug to fill the contact hole.

14. (Currently amended) The method as claimed in claim 13, wherein in the step (a), a device isolation layer is formed in a resist region,

wherein in the step (h), a resistor pattern is formed in the resist region,

wherein the ~~low resist conductive~~ high-conductivity layer, the second conductive layer, and the triple layer are removed in the contact region of the resistor pattern prior to formation of the interlayer insulating layer, and

wherein in the step (i), a contact hole is formed ~~to extend over only the~~ in a contact region of the resistor pattern in the resist region.

15. (Currently amended) The method as claimed in claim 13, wherein the removal region includes a resist region,

wherein in the step (h), a resistor pattern is formed in the resist region,

wherein the high-conductivity layer is removed ~~in all regions of~~ from the resistor pattern prior to formation of the interlayer insulating layer, and

wherein in the step (i), a contact hole is formed in the resist region to expose the first conductive layer.

16. (Currently amended) A method of fabricating a non-volatile semiconductor memory device, comprising:

(a) forming a low-voltage gate insulating layer in at least a peripheral low-voltage region of the substrate, and forming a high-voltage-type gate insulating layer in at least a peripheral high-voltage region of the substrate;

(b) stacking a first conductive layer on an entire surface of the substrate;

(c) removing the first conductive layer in the cell array region to expose the substrate;

(d) sequentially forming a triple layer and a second conductive layer over substantially ~~the~~an entire surface of the ~~exposed~~ substrate where the first conductive layer in the cell array region is removed, the triple layer including a tunneling insulating layer, a charge storage layer, and a blocking insulating layer;

(e) patterning a substrate where the second conductive layer is formed, whereby removing the second conductive layer and the triple layer in a removal region including the peripheral low-and high-voltage regions;

(f) forming a trench type device isolation layer in a substrate undergoing the step (e);

(g) forming a high-conductivity layer over substantially the entire surface of the substrate where the device isolation layer is formed;

(h) patterning the substrate where the ~~low resist~~ high-conductiveity layer ~~is formed~~, thereby forming a cell gate pattern in the cell array region and forming high-and low-voltage-type gate patterns in the peripheral high-and low-voltage regions, respectively.

(i) forming and patterning an interlayer insulating layer on an entire surface of the substrate to form contact holes including contact holes exposing the high-conductivity layer; and

(j) forming a contact plug to fill the contact hole.

17. (Currently amended) The method as claimed in claim 16, wherein in the step (a), the gate insulating layer is formed in a resist region,

wherein in the step (h), a resistor pattern is formed in the resist region,

wherein the high-conductivity layer, the second conductive layer, and the triple layer are removed in ~~the~~ a contact region of the resistor pattern prior to formation of the interlayer insulating layer, and

wherein in the step (i), only a contact hole ~~stretching over~~ in the contact region of the resistor pattern is formed in the resist region.

18. (Original) The method as claimed in claim 16, further comprising forming an insulating spacer on sidewalls of the patterns formed in the step (h).

19. (Currently Amended) The method as claimed in claim 16, wherein the ~~low-resist conducive~~ high-conductivity layer is formed by sequentially stacking a conductive layer of silicon and another conductive layer of metal.

20. (Currently Amended) The method as claimed in claim 19, wherein in the step (f), a device isolation layer is formed in a resist region,

wherein in the step (h), a resistor pattern comprising the high-conductivity layer is formed in the resist region,

wherein ~~a~~ another conductive layer of metal ~~containing conductive layer~~ is removed in all regions of the resistor pattern prior to formation of the interlayer insulating layer, and

wherein in the step (i), a contact hole is formed in the resist region to expose the ~~polysilicon~~ conductive layer of silicon.

21. (Currently Amended) The method as claimed in claim 16, wherein the removal region includes a resist region,

wherein in the step (h), a resistor pattern is formed in the resist region,

wherein the high-conductivity layer is removed ~~in all regions of~~ from the resistor pattern prior to formation of the interlayer insulating layer, and

wherein in the step (i), a contact hole is formed in the resist region to expose the first conductive layer.